Application Note	THAN0123_Rev.1.10_E

THC63LVDM87
Application Note
System Diagram and PCB Design Guide Line

Date	Revision
20120406	THAN0123_Rev.1.00_E
20120620	THAN0123_Rev.1.10_E

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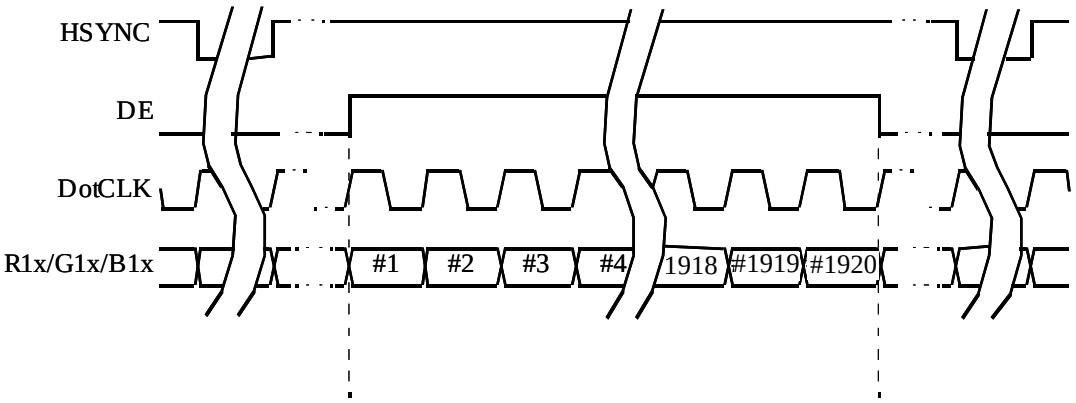
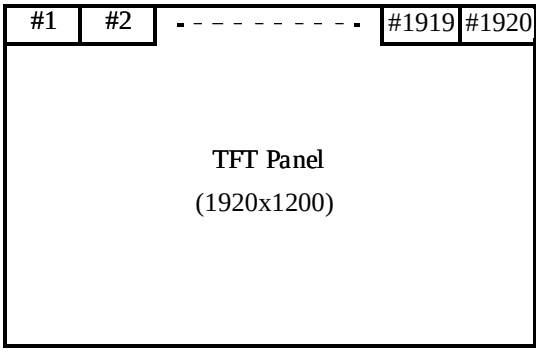
1. CMOS/TTL Data Timing Diagram

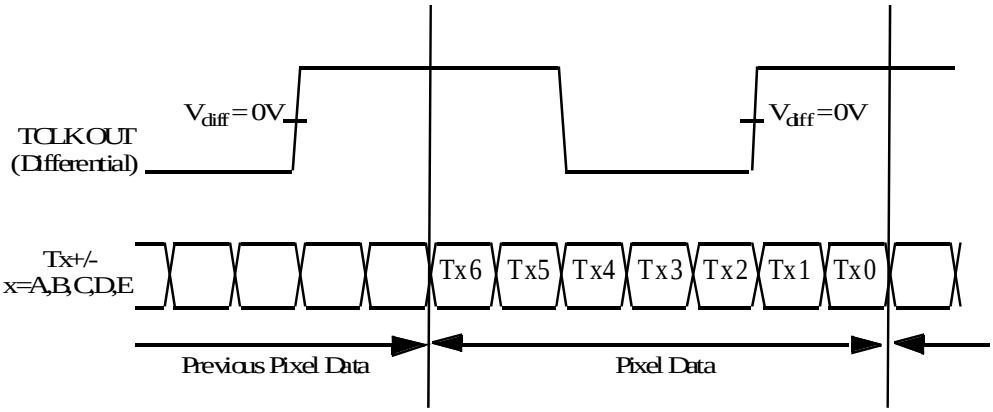




Note :

	Red	Green	Blue
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
6Bit LSB	R2	G2	B2
	R1	G1	B1
8Bit LSB	R0	G0	B0

2. LVDS Data Timing Diagram



THC63LVDM87 Pixel Data Assign _ JEITA (6bit, 8Bit Application)

	6Bit	8Bit
TA0	R2	R2
TA1	R3	R3
TA2	R4	R4
TA3	R5	R5
TA4	R6	R6
TA5	R7	R7
TA6	G2	G2
TB0	G3	G3
TB1	G4	G4
TB2	G5	G5
TB3	G6	G6
TB4	G7	G7
TB5	B2	B2
TB6	B3	B3
TC0	B4	B4
TC1	B5	B5
TC2	B6	B6
TC3	B7	B7
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	-	R0
TD1	-	R1
TD2	-	G0
TD3	-	G1
TD4	-	B0
TD5	-	B1
TD6	-	N/A

Note : For 6Bit application use A to C channel and open TD+/- pin.

THC63LVDM87 Pixel Data Assign _VESA (6bit, 8Bit Application)

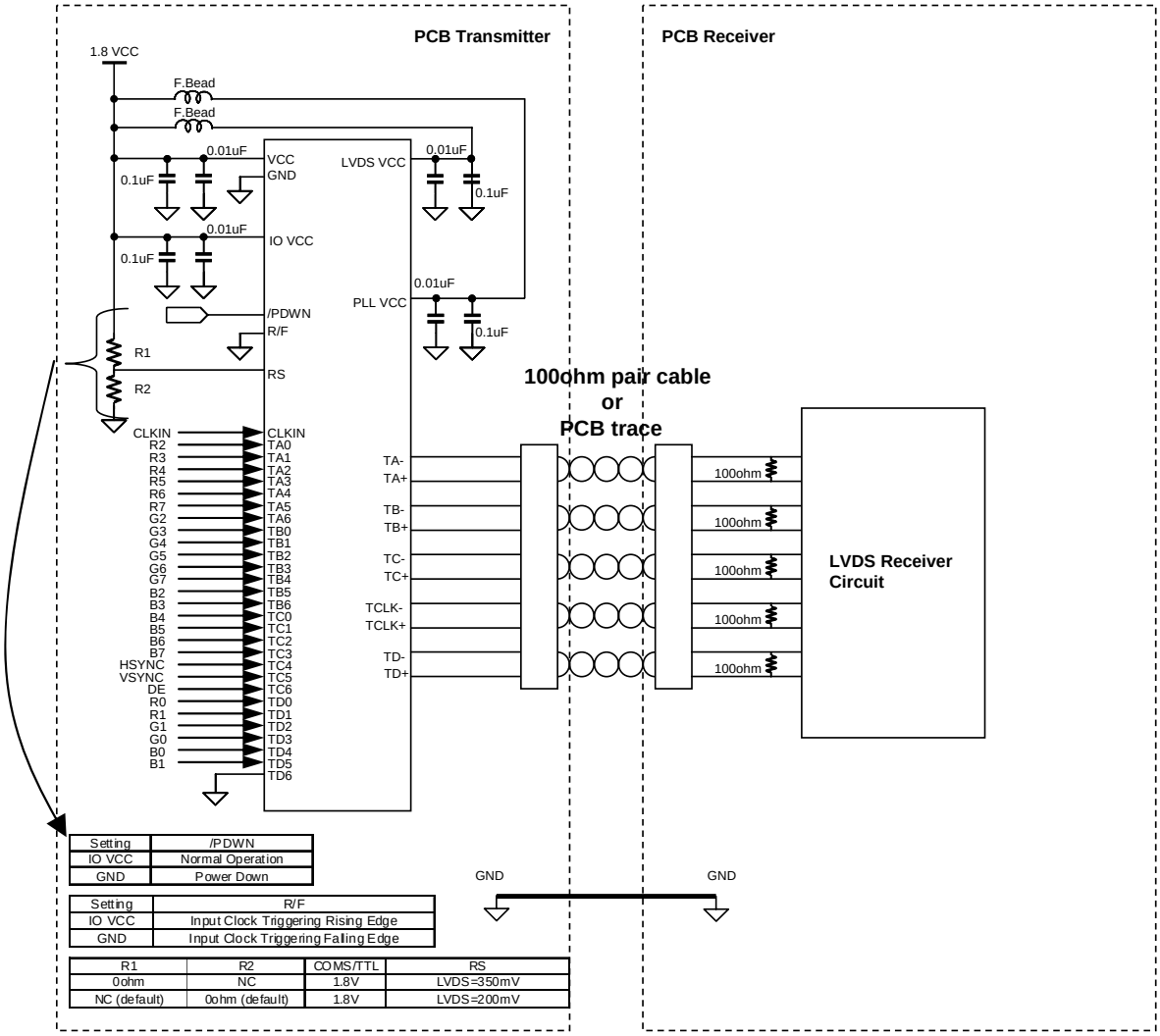
	6Bit	8Bit
TA0	R0	R0
TA1	R1	R1
TA2	R2	R2
TA3	R3	R3
TA4	R4	R4
TA5	R5	R5
TA6	G0	G0
TB0	G1	G1
TB1	G2	G2
TB2	G3	G3
TB3	G4	G4
TB4	G5	G5
TB5	B0	B0
TB6	B1	B1
TC0	B2	B2
TC1	B3	B3
TC2	B4	B4
TC3	B5	B5
TC4	Hsync	Hsync
TC5	Vsync	Vsync
TC6	DE	DE
TD0	-	R6
TD1	-	R7
TD2	-	G6
TD3	-	G7
TD4	-	B6
TD5	-	B7
TD6	-	N/A

Note : For 6Bit application use A to C channel and open TD+/- pin.

3. Example of System Diagram

1) 8 bit 1.8V CMOS/TTL Input

THC63LVDM87 Setting : Falling edge / Normal swing / JEITA mapping



Setting	/PDWN
IO VCC	Normal Operation
GND	Power Down

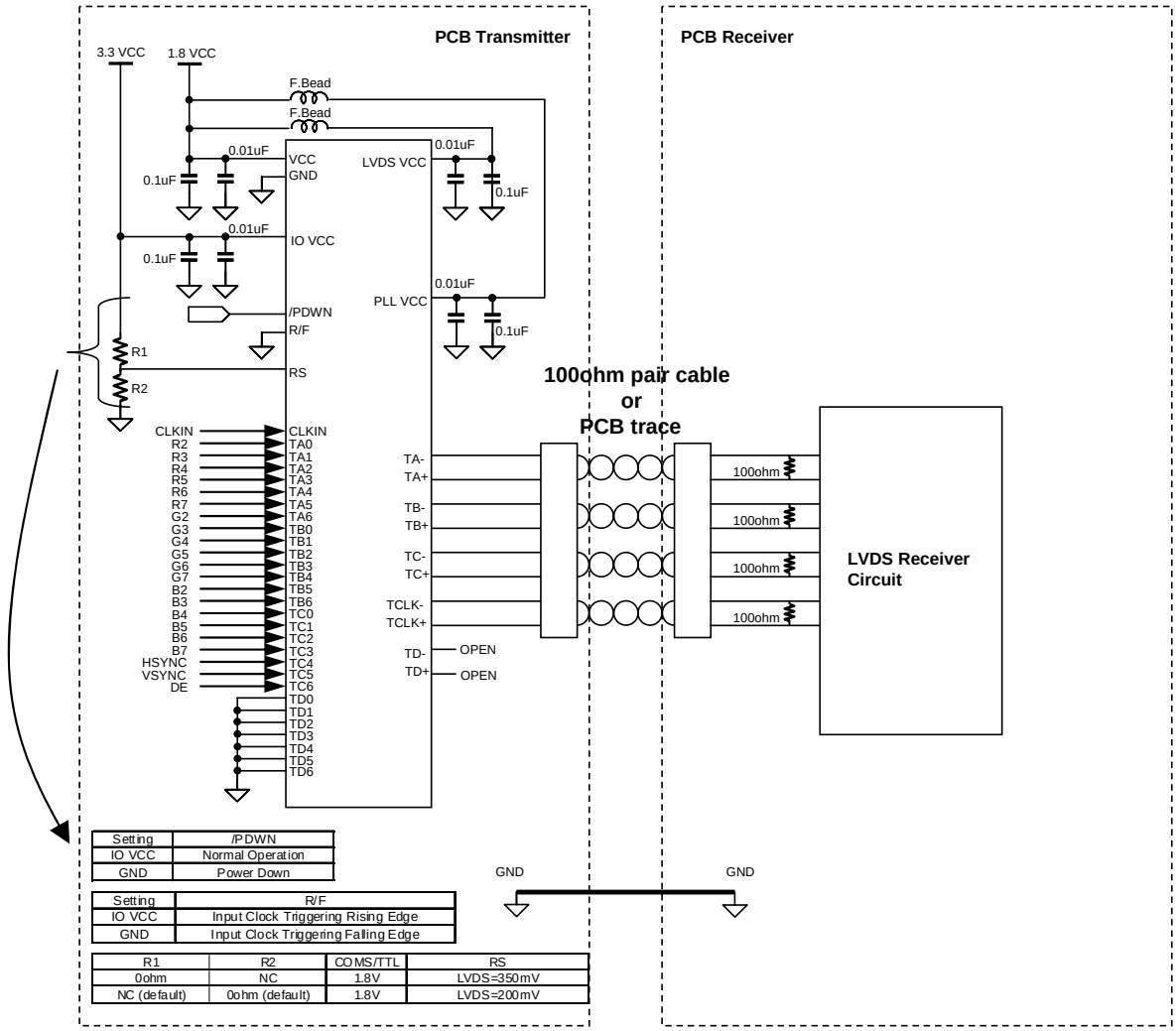
Setting	R/F
IO VCC	Input Clock Triggering Rising Edge
GND	Input Clock Triggering Falling Edge

R1	R2	COMS/TTL	RS
0ohm	NC	1.8V	LVDS=350mV
NC (default)	0ohm (default)	1.8V	LVDS=200mV

Note :

- Regarding the /PDWN, please use switching if needed.
- Regarding the R/F and RS pin, please select VCC level or GND level it depends on user operation.
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.
- Connect each Board GND
- COMS/TTL input pin that not in use, it must be tied to GND.

2) 6 bit 3.3V CMOS/TTL Input
THC63LVDM87 Setting : Falling edge / Normal swing / JEITA mapping



Note :

- Regarding the /PDWN, please use switching if needed.
- Regarding the R/F and RS pin, please select VCC level or GND level it depends on user operation.
- Please prepare the 100ohm pair cable or PCB pattern trace that is controlled with 100ohm for LVDS signal.
- Connect each Board GND
- COMS/TTL input pin that not in use, it must be tied to GND.

4. Note

4.1) Cable Connection and Disconnection

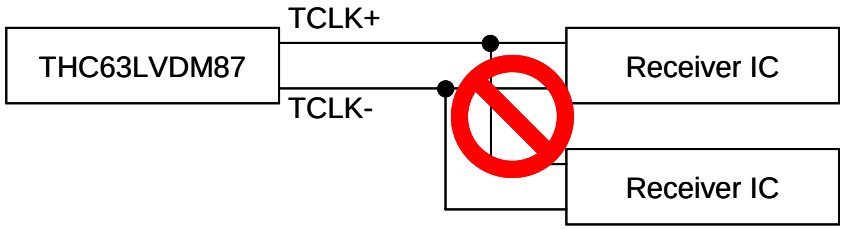
Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

4.2) GND Connection

Connect the each GND of the Board which THC63LVDM87 and Receiver on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

4.3) Multi Drop Connection

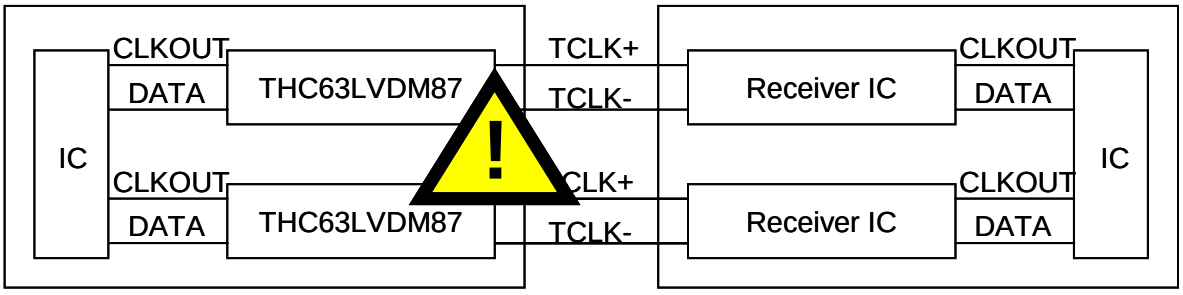
Multi drop connection is not recommended.

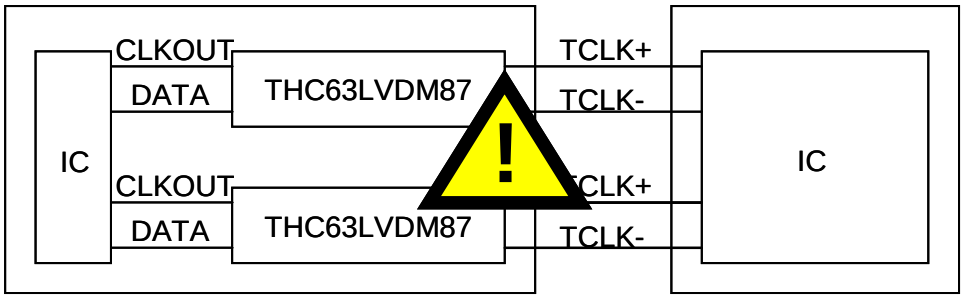


4.4) Asynchronous use

Asynchronous uses such as following systems are not recommended. If it's not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

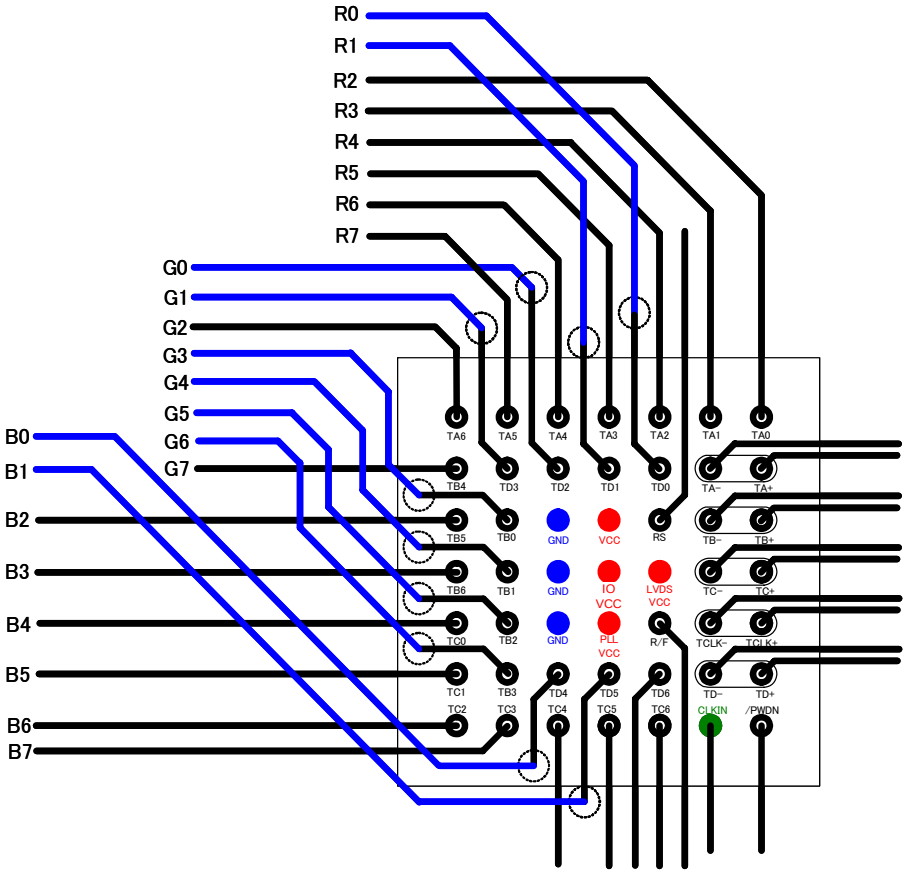




5. Trace Example for BGA

TOP VIEW

	1	2	3	4	5	6	7	
A	TA6	TA5	TA4	TA3	TA2	TA1	TA0	A
B	TB4	TD3	TD2	TD1	TD0	TA-	TA+	B
C	TB5	TB0	GND	VCC	RS	TB-	TB+	C
D	TB6	TB1	GND	IO VCC	LVDS VCC	TC-	TC+	D
E	TC0	TB2	GND	PLL VCC	R/F	TCLK-	TCLK+	E
F	TC1	TB3	TD4	TD5	TD6	TD-	TD+	F
G	TC2	TC3	TC4	TC5	TC6	CLKIN	/PWDN	G
	1	2	3	4	5	6	7	



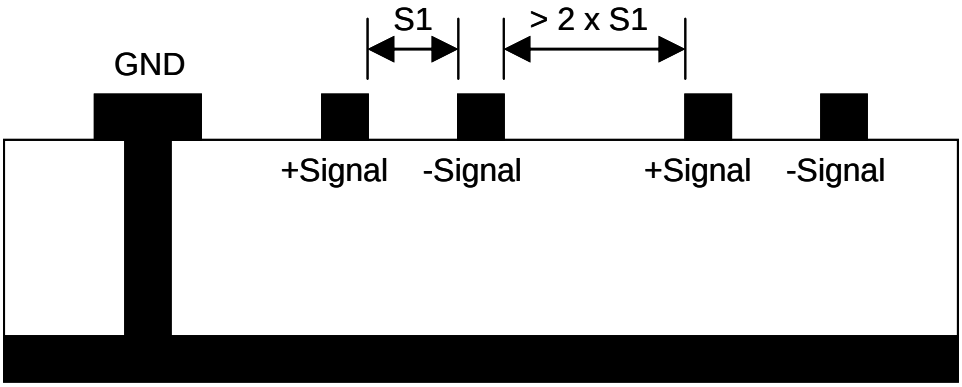
6. PCB Design Guide Line

General Guideline

- Use 4 layers PCB (minimum).
- Locate by-pass capacitors adjacent close to the device pins to a maximum extent.
- Make the loop minimum which is consist of Power line and GND line.
- Use large GND plane.
- Separate VDD power supply for each block via ferrite bead.

LVDS Trace

- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector and cable) should be well balanced. (Keep all these differential impedance and the length of media as same as possible)
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection. See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away as possible.
- Avoid 90 degree bends and sharp angles.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, cable and termination to minimize reflections (emissions) for cabled applications (typically 100ohm differential mode characteristic impedance).
- Place terminal resistor close to the Receiver pins to a maximum extent.
- To place common mode choke coil is desired for EMI reduction.



Notices and Requests

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