THM3561

Stepping Motor Driver with LVDS Interface

Overview

THM3561 is a motor driver for driving a unipolar stepping motor. It contains four built-in high-voltage and low on-resistance transistors and these are controlled by writing a setting register by a serial interface.

LVDS transmission is possible in the serial interface, therefore; it achieves high noise resistance, high speeds and long-distance transmission. To return a sensor signal for position detection, THM3561 contains a built-in serial interface. It is possible to significantly reduce the number of parts.

The arrangement of the motor driver and the high flexibility of the connection are possible as the serial interface is used to register reading, which corresponds to the cascade connection and multi-drop.

As it is a simple communication protocol, it reduces the load on the CPU and can be easily controlled.

This product will operate at 5V using a built-in regulator, however a 3.3V system microcontroller can be directly connected by supplying 3.3V to the VIO pin.

It is possible to have a built-in clamp diode to the driver output, and to reduce the number of parts. The design of the damper circuit can be easily performed.

Application

- Amusement device
- Multi-functional printer (OA device)
- Industrial equipment, monitoring camera, etc.

Features

<Motor driver unit>
- 2-phase stepping motor driver
- Unipolar constant voltage drive
- Maximum output current 1.5A/phase (Tj=25˚C)
- Maximum output voltage 48V (recommended 45V)
- Phase input mode and clock input mode can be selected by a setting pin

<Serial interface>
- Maximum serial clock frequency 10Mbps
- Single-end transmission and LVDS transmission can be selected
- Bridge function from 4-wire CMOS level to LVDS
- Repeater function of LVDS with waveform and timing correction
- Maximum device address : 30
- Writing of all device batch registers is also possible
- Built-in 4-bit parallel-serial conversion function for sensor connection.

<Other>
- Various built- protection functions (UVLO, OCP and TSD)
- Fault detect output (OCP and TSD)
- Input voltage range 8V to 45V, absolute maximum rating: 48V
- Built-in regulator for internal power supply generation 5V
- package: QFN48 (7mm x 7mm)
- RoHS directive compliant

Use Case Diagram

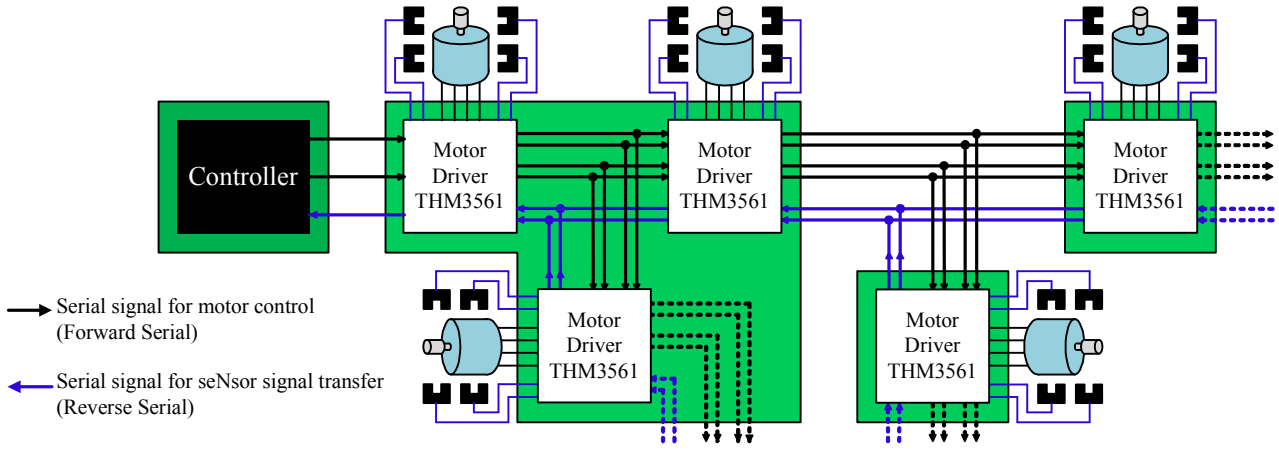


Figure 1. Use Case Diagram

Block Diagram

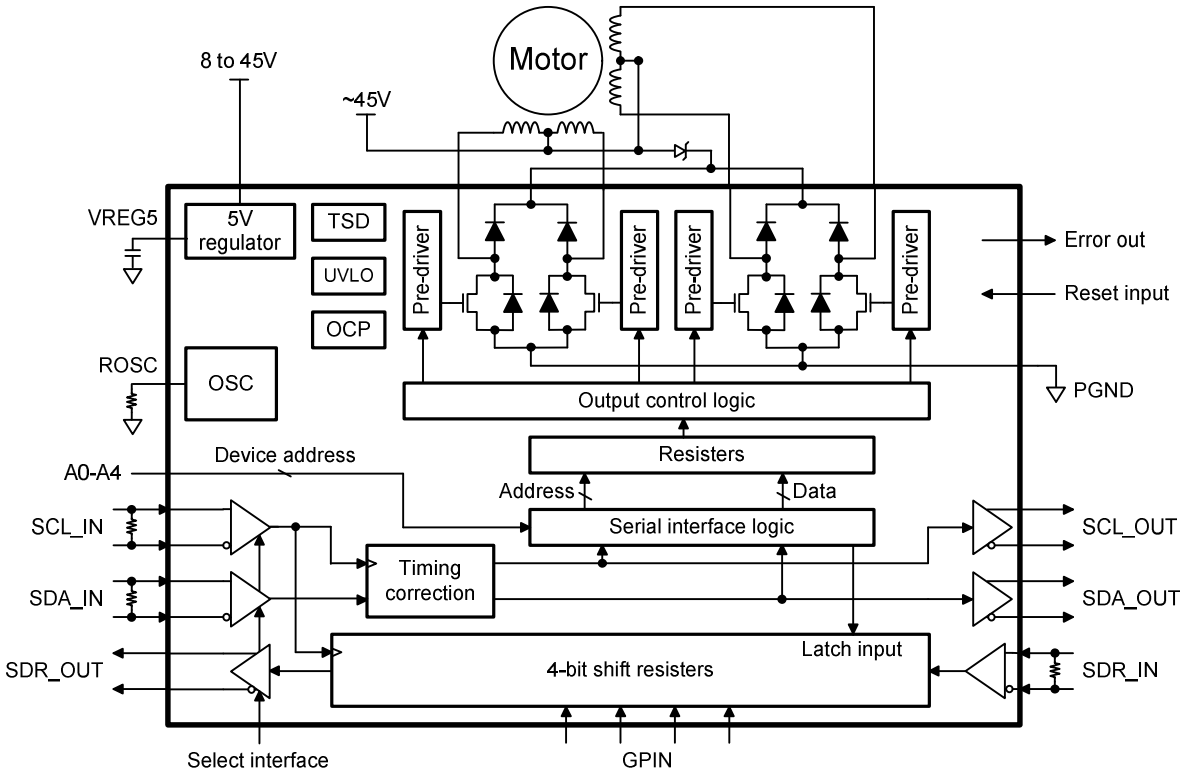


Figure 2. Block Diagram

Pin Configurations

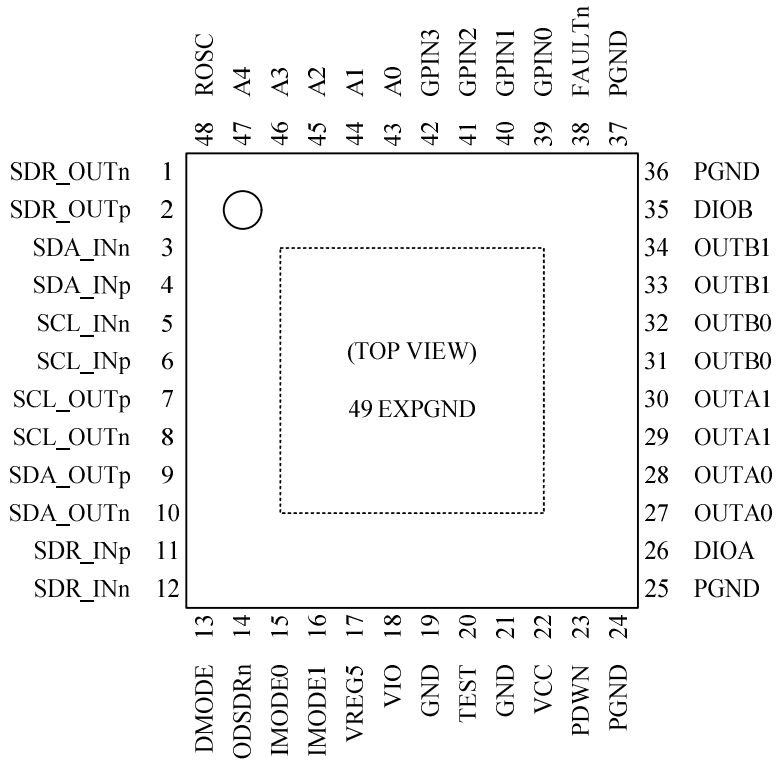


Figure 3. Pin Configurations

Pin List

Table 1. Pin Overview

Pin name	Pin number	Type[*1]	Description
SDR_OUTn	1	CLO	Serial signal output for sensor signal transfer (Reverse-Serial)
SDR_OUTp	2		
SDA_INn	3	CLI	Serial data input for motor control (Forward-Serial)
SDA_INp	4		
SCL_INn	5		Serial clock input for motor control (Forward-Serial)
SCL_INp	6		
SCL_OUTp	7	CLO	Serial clock output for motor control (Forward-Serial)
SCL_OUTn	8		
SDA_OUTp	9		Serial data output for motor control (Forward-Serial)
SDA_OUTn	10		
SDR_INp	11	CLI	Serial signal input for sensor signal transfer (Reverse-Serial)
SDR_INn	12		
DMODE	13	IN	Driver operation select mode High: clock input mode Low: Phase input mode For details, refer to “Driver operation mode”
ODSDRn	14	IN	Sensor signal output select High: push-pull output Low: open drain output
IMODE0	15	IN	Interface select For details, refer to “Interface pin setting”
IMODE1	16	IN	Interface select For details, refer to “Interface pin setting”
VREG5	17	IN	Internal LDO output (Typ. 5V) This pin usually gets connected to 4.7uF capacitor
VIO	18	PS	I/O power supply for interface input This pin usually gets connected to VREG5. This pin should be connected to a 3.3V power supply when you want to use the input directly from a 3.3V series host (microcomputer.)
TEST	20	-	This pin must be connected to Low level
VCC	22	PS	Connect to power supply
PDWN	23	IN	Power down input High: Low power state and internal logic reset Low: Normal operation
DIOA	26	OM	High-side clamp diode A-phase output (A-phase $\overline{\text{A}}$-phase common and cathode-side)
OUTA0	27,28	OM	A-phase output
OUTA1	29,30	OM	$\overline{\text{A}}$-phase output
OUTB0	31,32	OM	B-phase output
OUTB1	33,34	OM	$\overline{\text{B}}$-phase output
DIOB	35	OM	High-side clamp diode B-phase output (B-phase, $\overline{\text{B}}$-phase common and cathode-side)
FAULTn	38	OD	Fault detect output (OCP, TSD) Low: Fault detect / High-Z: Normal It will become an open-drain output. This pin is usually connected to 5V/3.3V with 1kohm or more pull-up resistor.
GPIN0-3	39,40,41,42	IN	General purpose digital input (Sensor signal input)
A0-4	43,44,45,46,47	IN	Device address input Bit 0-4

Pin List (continued)

Table 2. Pin Overview (continued)

Pin name	Pin number	Type*1	Description
ROSC	48	IN	Internal oscillator frequency setting Connect 47komh resistance between this pin and reference potential
PGND	24,25,36,37	PS	Power ground
GND	19,21	PS	Ground
EXPGND	49	PS	Exposed pad（Ground）

*1: CLO = CMOS level or LVDS output, CLI = CMOS level or LVDS input, PS = Power supply,
OD = Open drain output, OM = Motor drive output, IN = control input

Interface Mode Pin Setting

The #3_SDA_INn pin changes to "**OMODE**" pin (name) when used with 3-wire or 4-wire CMOS inputs

The interface mode of the serial signal for motor control and serial signal for sensor signal transfers can be selected by setting IMODE1, IMODE0 pin and OMODE pin. Set as described in the following table depending on the connection point.

・Name of serial signal pin for motor control and name of serial signal for sensor signal transfer mentioned in the pin list are the pin names at the time of LVDS I/O setting.

・The #5_SCL_INn pin should be connected to "Low" level, if it uses a 3-wire CMOS input.

Table 3. Interface Mode Setting

Description	Pin#	LVDS input (IMODE0=H / IMODE1=L)	3-wire CMOS input (IMODE0=L / IMODE1=H)		4-wire CMOS input (IMODE0=H / IMODE1=H)	
		LVDS output	LVDS output (OMODE=L)	3-wire CMOS output (OMODE=H)	LVDS output (OMODE=L)	3-wire CMOS output (OMODE=H)
Serial signal for the motor control (Forward-Serial)						
Data input	3	SDA_INn (Diff.-)	**OMODE（for details on High/Low settings, refer to the above mentioned）**			
	4	SDA_INp (Diff.+)	SDA_IN		SI	
Clock input	5	SCL_INn (Diff.-)	**This should be connected to Low level, if it uses a 3-wire CMOS input**		CSn	
	6	SCL_INp (Diff.+)	SCL_IN		SCK	
Data output	7	SCL_OUTp (Diff.+)	SCL_OUTp	SCL_OUT	SCL_OUTp	SCL_OUT
	8	SCL_OUTn (Diff.-)	SCL_OUTn	(NC)	SCL_OUTn	(NC)
Clock output	9	SDA_OUTp (Diff.+)	SDA_OUTp	SDA_OUT	SDA_OUTp	SDA_OUT
	10	SDA_OUTn (Diff.-)	SDA_OUTn	(NC)	SDA_OUTn	(NC)
Serial signal for sensor signal transfer (Reverse-Serial)						
Output	1	SDR_OUTn(Diff.-)	(NC)			
	2	SDR_OUTp(Diff.+)	SO			
Input	11	SDR_INp(Diff.+)	SDR_INp	SDR_IN	SDR_INp	SDR_IN
	12	SDR_INn(Diff.-)	SDR_INn	(NC)	SDR_INn	(NC)

Absolute Maximum Rating *

Table 4. Absolute Maximum Rating

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	VCC supply voltage	-	-0.4	48	V
V_{OUT}	Driver output pin voltage	-	-0.4	48	V
V_{DIO}	Diode output pin voltage	-	-0.4	48	V
V_{RDIO}	High-side diode reverse voltage	-	-	48	V
I_{MOT}	Driver output current	Tj=25deg.	Limited by OCP function		A/phase
$I_{F(PEAK)}$	High-side diode forward current (Peak)	Tj=25deg. ,t<1us	-	1.8	A/phase
$I_{F(RMS)}$	High-side diode forward current (RMS)	-	-	1.2	A/phase
VIO	Interface supply voltage	-	-0.5	6.0	V
V_{DIN}	Digital input voltage	-	-0.5	6.0	V
P_D	Power dissipation	Ta=25 deg.	-	4.4	W
T_{STG}	Storage temperature	-	-55	150	deg.
T_j	Junction temperature	-	-	150	deg.

* "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" specify conditions for device operation.

Recommended Operation Conditions

Table 5. Recommended Operation Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	VCC supply voltage	-	8	45	V
V_{OUT}	Driver output pin voltage	-	-0.3	45	V
V_{DIO}	Diode output pin voltage	-	-0.3	45	V
V_{RDIO}	High-side diode reverse voltage	-	-	45	V
VIO	Interface supply voltage	-	3.0	VREG5+0.3	V
V_{DIN}	Digital input voltage (VREG5)	-	-0.3	5.5	V
	Digital input voltage (VIO)	-	-0.3	VIO+0.3	V
$I_{OUT(PEAK)}$	Driver output current (Peak) one phase	T_j=25deg.,t<1us	-	1.5	A/phase
	Driver output current (Peak) total phase	T_j=25deg.,t<1us	-	2.0	A
$I_{OUT(RMS)}$	Driver output current (RMS) one phase	T_j=25deg.	-	1.2	A/phase
	Driver output current (RMS) total phase	T_j=25deg.		1.6	A
I_F	High-side diode forward current (Peak)	T_j=25deg.,t<1us	-	1.2	A/phase
T_a	Operating ambient temperature	-	-40	85	deg.

Electrical Characteristics

Table 6. DC Specifications

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Vcc supply current	CMOS input (*1) CMOS output (*2)	-	-	25	mA
		LVDS input (*1) LVDS output (*3)	-	-	40	mA
I_{CCS}	Power down current	PWDN=High	-	-	100	uA
V_{THUVLO}	UVLO threshold (VCC: L→H)	-	7.0	7.5	8.0	V
V_{DUVLO}	UVLO hysteresis	-	-	0.5	-	V
R_{ON}	Driver output ON resistance	T_j=25deg., I_{OUT}=700mA	-	0.55	-	ohm
		T_j=85deg., I_{OUT}=700mA	-	0.8	-	ohm
I_{OFF}	Driver output leak current	T_j=25deg.	-	-	10	uA
V_F	High-side diode forward voltage	I_f=700mA	-	2.5	-	V

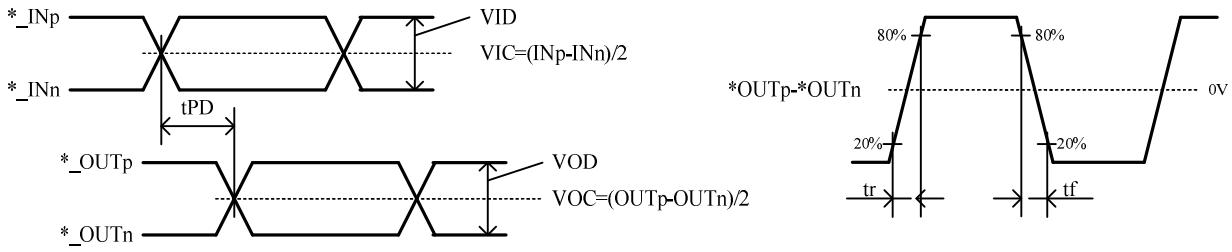
Electrical Characteristics (continued)

Table 7. DC Specifications (continued)

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_R	High-side diode reverse leak current	T_j=25deg.	-	-	10	uA
		T_j=150deg.	-	-	5	mA
I_{OCP}	Over current detection level	-	2.0	2.5	3.2	A
VREG5	Internal regulator output voltage	I_O = 0 to 50mA	4.5	-	5.5	V
$V_{IH(VREG5)}$	Digital input high level voltage (VREG5 system)	Except the PWDN	4.0	-	-	V
$V_{IL(VREG5)}$	Digital input low level voltage (VREG5 system)	Except the PWDN	-	-	1.0	V
$V_{IH(VIO)}$	Digital high level voltage (VIO system)	VIO=VREG5	4.0	-	-	V
		VIO=3.3V	2.8	-	-	V
$V_{IL(VIO)}$	Digital low level voltage (VIO system)	VIO=VREG5	-	-	1.0	V
		VIO=3.3V	-	-	0.8	V
I_{IDIG}	Digital input leak current	-	-	-	±10	uA
$V_{IH(PDWN)}$	PDWN input high level voltage	-	4.0	-	-	V
$V_{IH(PDWN)}$	PDWN input low level voltage	-	-	-	1.0	V
$V_{OH(VREG5)}$	Digital output high level voltage (VREG5 system)	I_{OL}=1mA	4.0	-	-	V
$V_{OL(VREG5)}$	Digital output low level voltage (VREG5 system)	I_{OL}=1mA	-	-	0.5	V
$V_{OH(VIO)}$	Digital output high level voltage (VIO system)	I_{OL}=1mA	VIO x 0.7	-	-	V
$V_{OL(VIO)}$	Digital output low level voltage (VIO system)	I_{OL}=1mA	-	-	VIO x 0.3	V
$V_{OL(FAULTn)}$	Open drain output low level voltage (FAULTn)	I_{OL}=1mA	-	0.55	1	V
V_{IDF}	LVDS input differential voltage	V_{IC}=1.2V	±100	-	-	mV
I_{IL}	LVDS input leak current	-	-	-	±30	uA
V_{ODF}	LVDS output differential voltage (SCL_OUT/SDA_OUT)	100ohm terminal	280	370	460	mV
	LVDS output differential voltage (SDR_OUT)	100ohm terminal	350	350	560	mV
V_{OC}	LVD output common voltage	-	1.1	1.21	1.4	V

(*1) Current will increase if internal regulator (VREG5) uses the external circuits.
(*2) No termination resistor.
(*3) It uses the SCL_OUT, SDA_OUT, SDR_OUT terminal resistor and 100ohm connection.



*_INp : SCL_Inp , SDA_Inp , SDR_INp
*_INn : SCL_INn , SDA_INn , SDR_INn
*_OUTp : SCL_OUTp , SDA_OUTp , SDR_OUTp
*_OUTn : SCL_OUTn , SDA_OUTn , SDR_OUTn

Figure 4. LVDS Specification

Electrical Characteristics (continued)

Table 8. AC Specifications

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
fOSC	Internal oscillator frequency	ROSC = 47kohm	1.2	1.6	2	MHz
tDOUT	Driver output delay time OFF→ON	Phase input mode	-	3.6	-	us
		Clock input mode	-	4.2	-	us
tDOUT	Driver output delay time ON→OFF	Phase input mode	-	3	-	us
		Clock input mode	-	3.6	-	us
tROUT	Driver output rise time	12V, 700mA, Resistance load 0% → 100% (*4)	-	125	-	ns
tFOUT	Driver output fall time	12V, 700mA, Resistance load 100% → 0% (*4)	-	140	-	ns
tOCP	OCP recovery time	-	-	1.28	-	ms

(*4) Driver output ON resistance x 700mA=0%, 12V=100%

Driver Output Timing

The setting is reflected to the driver output by the internal oscillator after write to register.
In the case of phase input mode, output is switched to the following post of time after write to register:
OFF→ON: about 3.6us (Typ.)
ON→OFF: about 3.0us (Typ.)
In the case of clock input mode, output is switched to the following post of time after write to register:
OFF→ON: about 4.2us (Typ.)
ON→OFF: about 3.6us (Typ.)
In the case of performing settings by which OFF→ON and ON→OFF are generated simultaneously at different output pins (for example, at the time of change-over of output at OUTA0 pin and OUTA1 pin of 2-phase excitation etc.), the delay difference of 2 outputs becomes dead time (this is when both terminals are turned OFF).

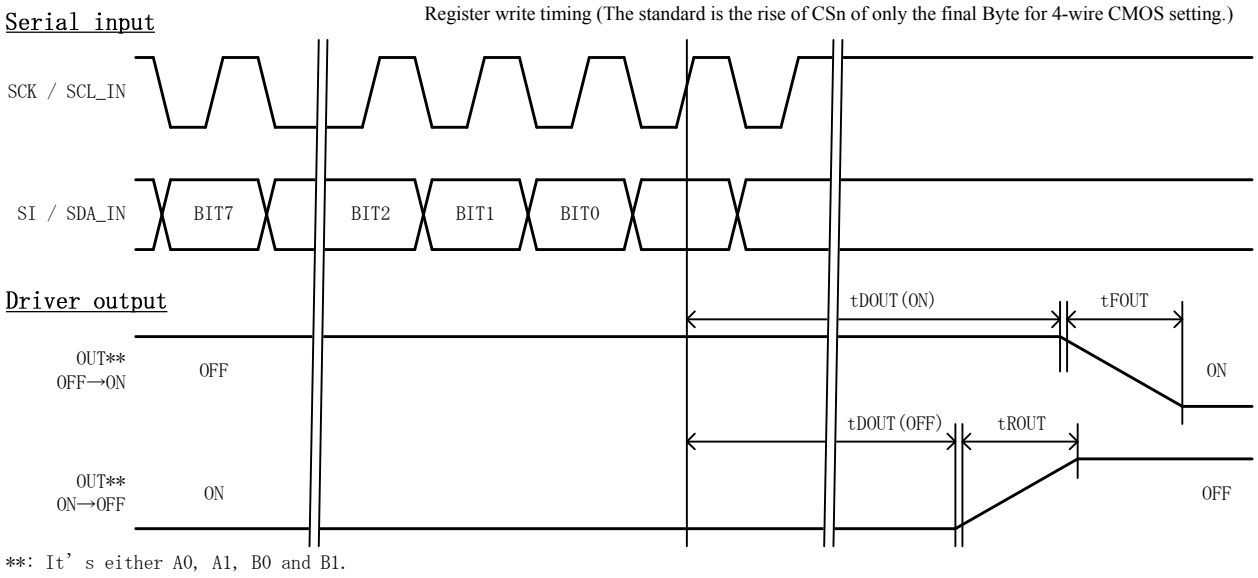


Figure 5. Output Driver Timing

Electrical Characteristics (continued)

Table 9. LVDS Specifications 1 (Forward-Serial input and Reverse-Serial output)

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
fSCL	SCL frequency (*5)	-	-	-	10	MHz
tDAH	SCL high time	-	40	-	-	ns
tDAL	SCL low time (*5)	-	50	-	-	ns
tSTAH	Header condition hold time	-	4	-	-	ns
tDSU	SDA setup time	-	4	-	-	ns
tDHO	SDA hold time	-	3	-	-	ns
tRDO	SDR_OUT output delay time (*5)	VIO=VREG5, 100ohm terminal	-	20	35	ns
tRRPT	SDR propagation delay time (*5)	VIO=VREG5, 100ohm terminal	-	10	20	ns

Table 10. LVDS Specifications 2 (Forward-Serial output and Reverse-Serial input)

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
tr, tf	SCL/SDA output rise and fall time	100ohm terminal	-	8	12	ns
tSTAH	Header condition hold time	-	6	10	20	ns
tDSU	SDA setup time	-	6	10	20	ns
tDHO	SDA hold time	-	5	-	-	ns
tRSU	SDR setup time	-	10	-	-	ns
tRHO	SDR hold time	-	10	-	-	ns
tPWE	End pulse width	-	25	40	70	ns
tPD	SCL propagation delay time	-	-	21	35	ns

(*5) This parameter is applicable to write a register and read sensor signals (shift register mode).
SCL frequency and SCL low time are limited by cascaded stages and wiring length if it use read sensor signal (address assign mode).

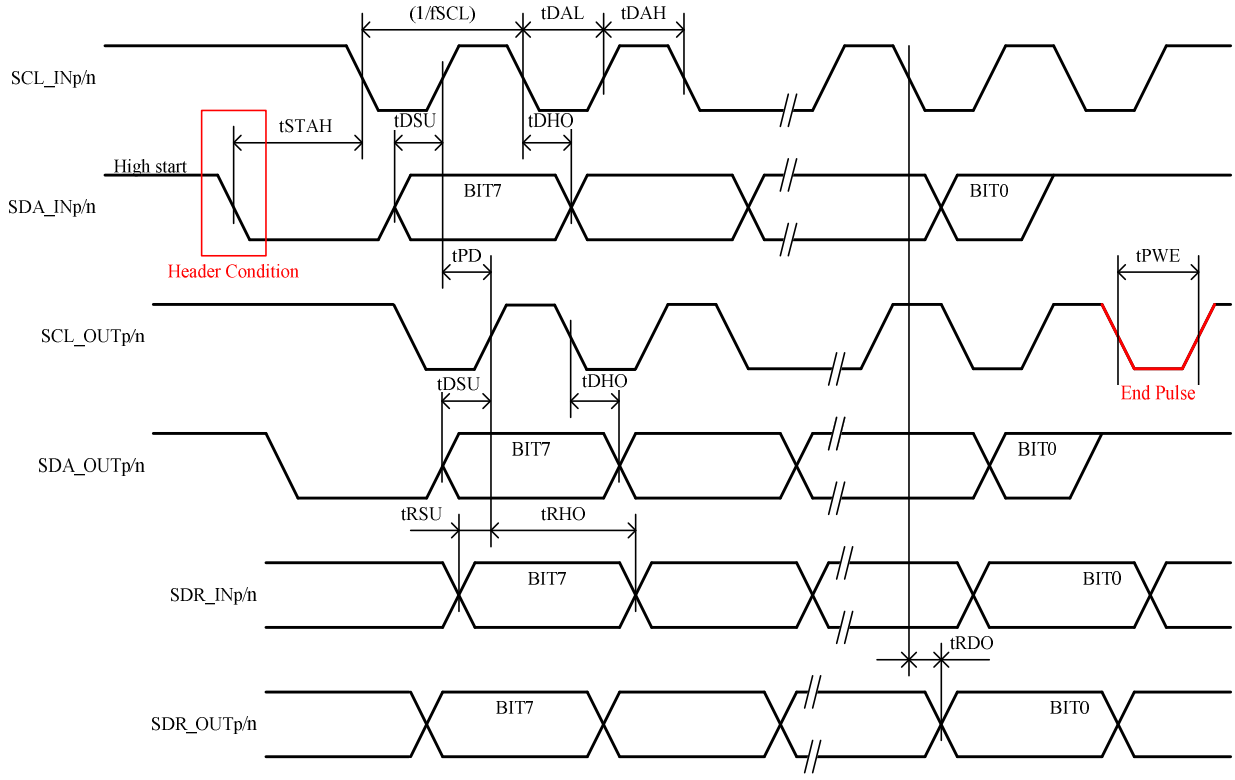


Figure 6. LVDS Timing Chart

Electrical Characteristics (continued)

Table 11. 3-wire CMOS Specifications 1 (Forward-Serial input and Reverse-Serial output)

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
fSCL	SCL frequency (*6)	-	-	-	10	MHz
tDAH	SCL high time	-	40	-	-	ns
tDAL	SCL low time (*6)	-	50	-	-	ns
tSTAH	Header condition hold time	-	4	-	-	ns
tDSU	SDA setup time	-	4	-	-	ns
tDHO	SDA hold time	-	3	-	-	ns
tRDO	SDR_OUT output delay time (*6)	VIO=VREG5, 100ohm terminal	-	21	35	ns
tRRPT	SDR propagation delay time (*6)	VIO=VREG5, 100ohm terminal	-	12	20	ns

Table 12. 3-wire CMOS Specifications 2 (Forward-Serial output and Reverse-Serial input)

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
tr, tf	SCL/SDA output rise and fall time	C=10pF	-	10	15	ns
tSTAH	Header condition hold time	-	6	10	20	ns
tDSU	SDA setup time	-	6	10	20	ns
tDHO	SDA hold time	-	5	-	-	ns
tRSU	SDR setup time	-	10	-	-	ns
tRHO	SDR hold time	-	10	-	-	ns
tPWE	End pulse width	-	25	40	70	ns
tPD	SCL propagation delay time	-	-	21	35	ns

(*6) This parameter is applicable to write a register and read sensor signals (shift register mode).
SCL frequency and SCL low time are limited by cascaded stages and wiring length if it use read sensor signal (address assign mode).

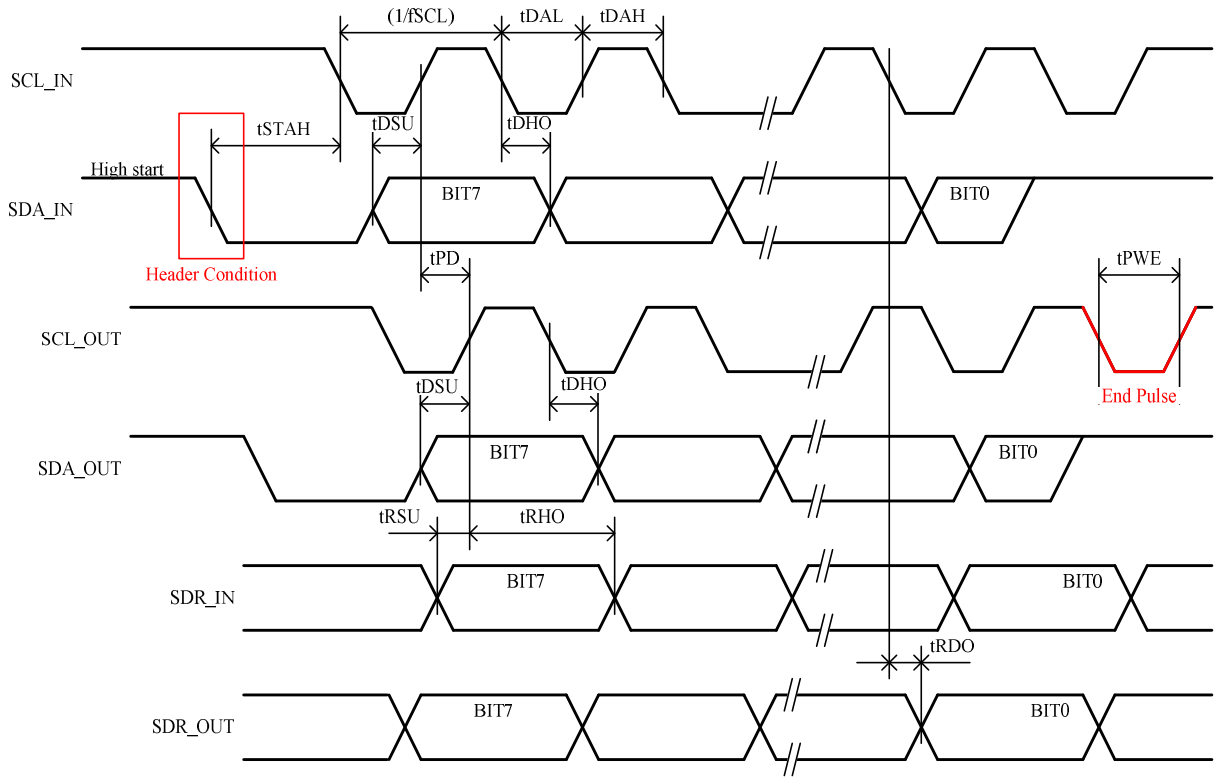


Figure 7. 3-wire CMOS Timing Chart

Electrical Characteristics (continued)

Table 13. 4-wire CMOS Specifications

Vcc=12V, Ta=25deg. unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
fSCK	SCK frequency (*7)	-	-	-	10	MHz
tCH	SCK high time	-	40	-	-	ns
tCL	SCK low time (*7)	-	50	-	-	ns
tDVCH	SI setup time	-	10	-	-	ns
tCHDX	SI hold time	-	10	-	-	ns
tCHSL	CSn not active hold time	-	40	-	-	ns
tSLCH	CSn active setup time	-	40	-	-	ns
tCHSH	CSn active hold time	-	40	-	-	ns
tSHCH	CSn not active setup time	-	40	-	-	ns
tSHSL	CSn not active time	-	200	-	-	ns
tROD	SO output delay time (*7)	VIO=VREG5	-	10.5	35	ns
tRRPT	SDR_IN/SO propagation delay time (*7)	VIO=VREG5	-	12.5	20	ns
		VIO=3.3V	-	15.4	25	ns

(*7) This parameter is applicable to write a register and read sensor signals (shift register mode).
SCL frequency and SCL low time are limited by cascaded stages and wiring length if it use read sensor signal (address assign mode).

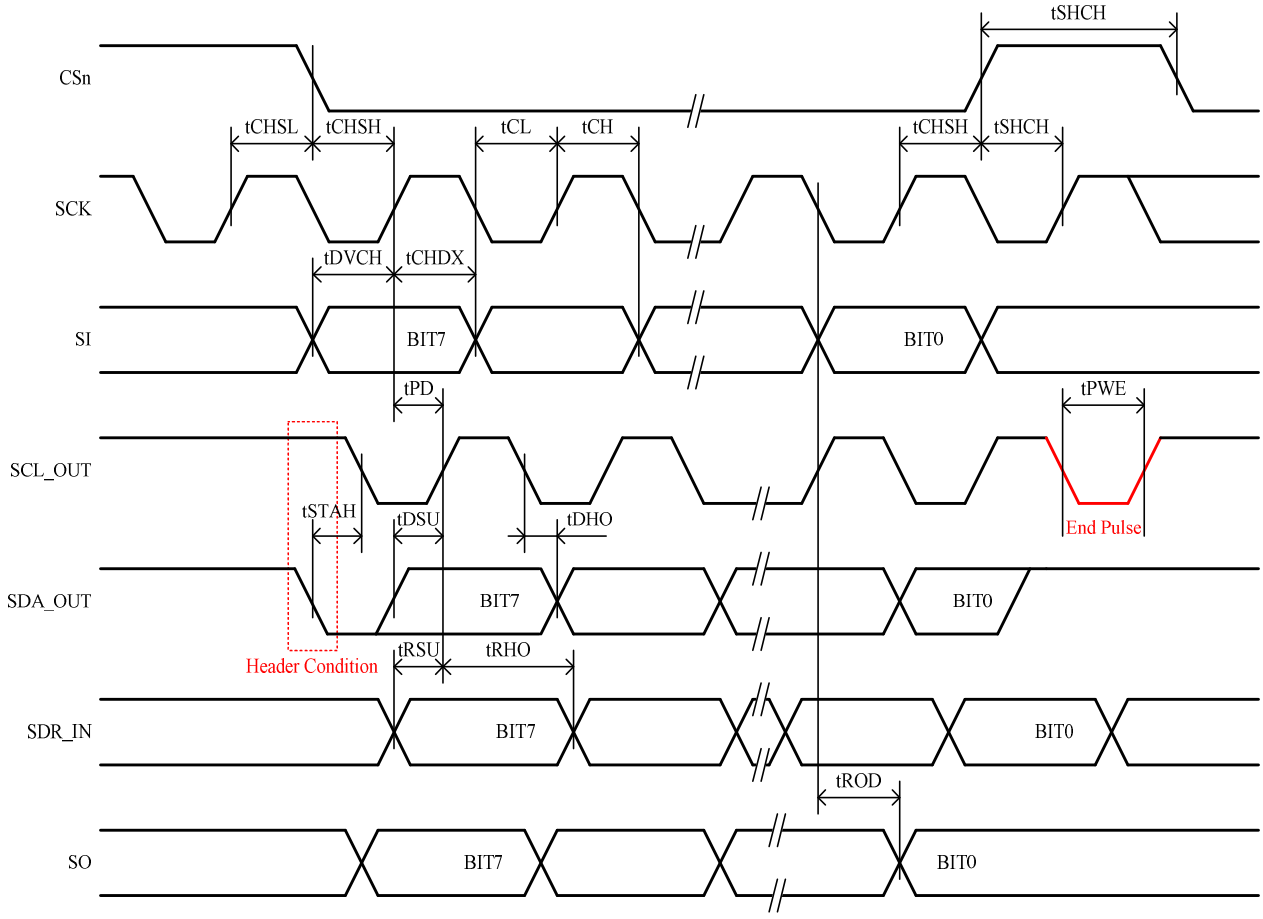


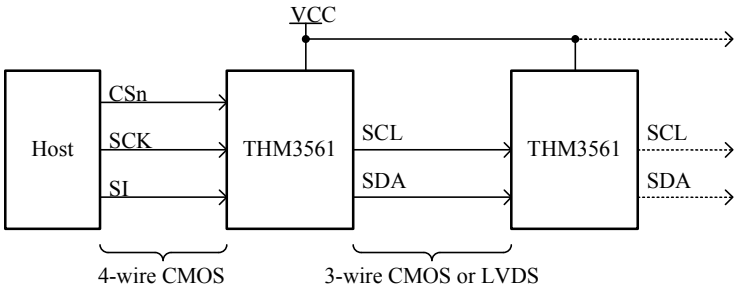
Figure 8. 4-wire CMOS Timing Chart

3-wire CMOS Input and LVDS Input Initialization

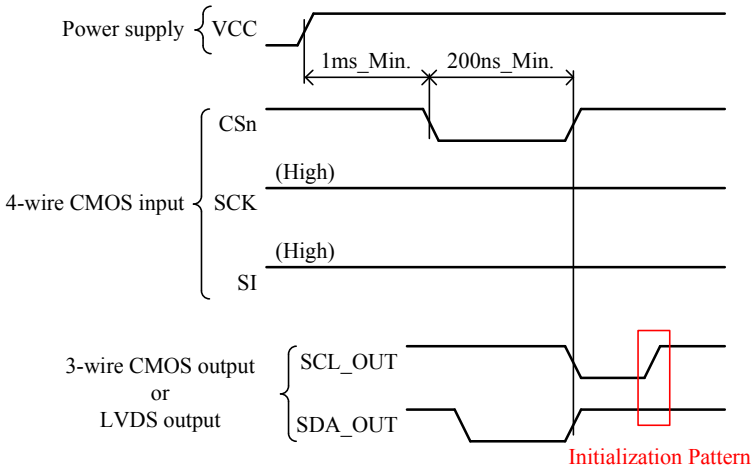
In the case of using 3-wire CMOS and LVDS input, perform the initialization before writing in the register after turning the power supply (VCC) on. If initialization is not performed, the first register writing ("1st Byte" to "Last Byte") may not be performed. Initialization is not needed if the first register writing is not required. In a case such as this continually refresh all the registers (R00-R18).

For performing the initialization, the initialization of the 3-wire CMOS and LVDS input is performed for all the devices that are connected in the post-stage, based on the input of pulse of Active-Low (pulse width: Min. 200ns) to CSn at the initial stage 4-wire CMOS input.

In the case of a cascade connection, a transmission delay time of a few minutes of the cascade stage is needed for completion of initialization of the 3-wire CMOS and LVDS.



Initialization Pattern (ex.1)
Low-active pulse input to the CSn pin.



Initialization Pattern (ex.2)
1st Byte(Device Address) =FFh input

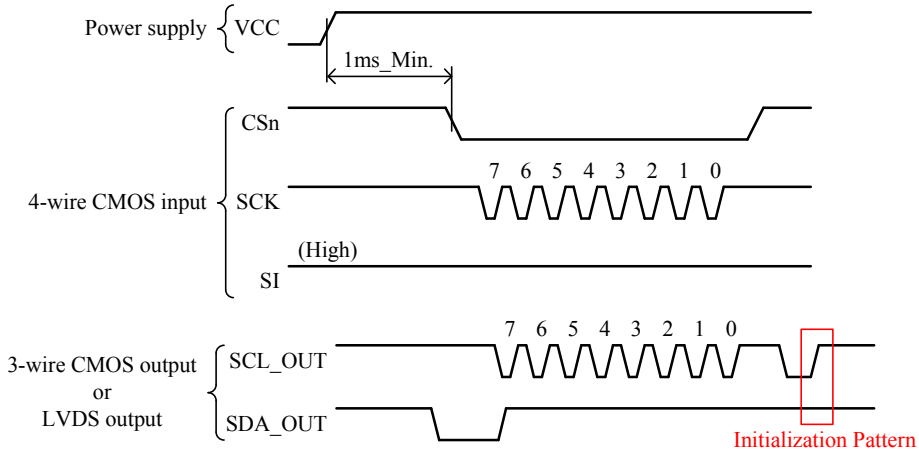


Figure 9. 3-wire CMOS Input and LVDS Input Initialization

Functional Description

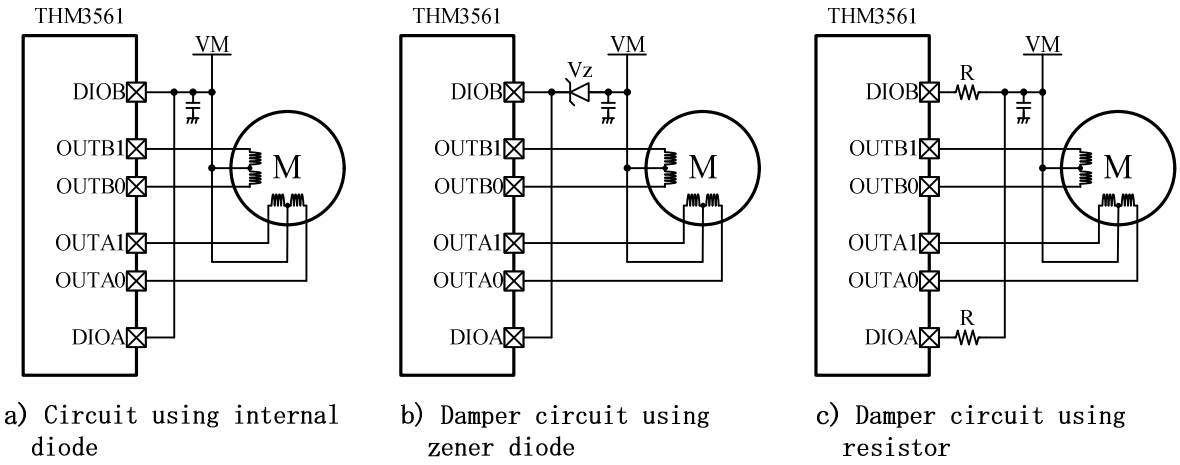
High-side clamp diode

This device contains clamp diode with high-side of each output driver.

Connect the DIOA pin and DIOB pin (cathode side of clamp diode) to the power supply of the motor in order to protect the output driver from reverse electricity by the driving of the inductor.

It is also recommended that the condenser of 1uF standard be connected to the VM line near the DIOA/DIOB pin of the driver, in order to prevent a rise in the clamp voltage due to fluctuations in the power supply of the motor (VM) due to power supply impedance.

As a configuration of clamp circuit, zener diode or a resistor may also be inserted between the DIOA pin, DIOB pin and power supply of the motor. In the case of using zener diode, take care that the sum of the motor V_z (zener voltage) and V_f of clamp diode (forward voltage) does not exceed the recommended operation range of the driver output pins (OUTA0 to OUTB1 pins) of this product. In the case of using the resistor, V_r that is determined by the product of motor current and resistance value is added to V_f and the motor voltage, instead of V_z. Take care that this value does not exceed the recommended operation range of the driver output pins (OUTA0 to OUTB1 pins) of this product.



a) Circuit using internal diode

b) Damper circuit using zener diode

c) Damper circuit using resistor

Figure 10. Example of High-side Clamp Circuit

[Calculation example] Condition: Motor voltage 12V / motor current 700mA

Vf = 2.5V (typ.)@700mA Hence, 45V (recommended operating voltage) > 12V + 2.5V + Vz.
Therefore, Vz< 30.5 V.

(The zener voltage is sometimes higher than the increase in the current in 2-phase excitation etc. Depending upon the configuration of the system side circuit. Keep adequate margins at the time of designing.)

Functional Description (continued)

Over Current Protection (OCP) and Blanking Function Setting.

This device contains an Over Current Protection (OCP) function. The output transistor stops if a current of more than 2.5A (typ.) flows through the output OUTA0 ~ OUTB1 pins (hereinafter, denoted as "OUT pin" in the case of showing all driver output pins). This time, phase A and B work independently. The correlation between the pin at which an over current has been detected and the pin at which the output stops is as given in table 14. This time, FAULTn pin outputs Low level.

Table 14. Over Current Detect Function

Over current detect	Output pins	
	OUTA0/OUTA1	OUTB0/OUTB1
OUTA0	OFF (Hi-Z)	Keep state
OUTA1	OFF (Hi-Z)	Keep state
OUTB0	Keep state	OFF (Hi-Z)
OUTB1	Keep state	OFF (Hi-Z)

The over current protection function automatically recovers after about 1.28ms (typ.) after becoming effective. At the time of automatic recovery, the FAULTn terminal stops Low level output and returns to High-Z output.

The blank function is the one by which the over current protection function becomes temporarily ineffective (mask) at the time of change-over, in order to prevent the incorrect operation of the over current protection function due to a spike current generated at the time of change-over of ON/OFF of the output driver. This function can be used by taking BLANK_EN bit of register as 1. Set the blank function effective as 1.

The blank time is different for OFF→ON and ON→OFF of the output transistor. At the initial stage (BLANK_SEL=0), OFF→ON time becomes 1CLK (0.625us, typ.) and ON→OFF time becomes 2CLK (1.25us, typ.) of the built-in oscillator. In the case of BLANK_SEL=1, the OFF→ON time becomes 3CLK (1.875us, typ.) and ON→OFF time becomes 4CLK (2.5us, typ.).

Thermal Shutdown (TSD)

This device contains a Thermal Shutdown (TSD) function. The OUT pin turns all channels OFF and the output of VREG5 stops when the junction temperature of the product rises further exceeding the absolute maximum rated value. This time, FAULTn pin outputs L level.

This function is designed for protection from smoke generation and fire and it actuates outside the absolute maximum rated value. Do the thermal designing while keeping an adequate margin so that this function does not actuate.

Under Voltage Lock Out (UVLO)

This device contains an Under Voltage Lock Out (UVLO) function for stable operation at the VCC and VREG5 pin.

This device stops operation when the VCC voltage falls below 7.5V (typ.), or VREG5 voltage falls below 3.5V (typ.).

Internal Regulator (VREG5)

This device contains a 5V (Typ.) output internal regulator (VREG5) for the internal circuit operation. VCC voltage is depressed to about 5V inside this LSI.

The VREG5 pin usually bypasses to GND with 4.7uF for normal operation.

In addition, the VREG5 pin can be supplied to some external circuits (ex. sensor).

Supply current is 50mA (Typ.)

The VREG5 pin bypasses to GND with 10uF if it used with an external circuit.

Functional Description (continued)

The internal circuit of this product operates on VREG5 voltage. However, in the case of using a host device of a 3.3V system (microcontroller etc.), the device can be directly connected to the pre-stage interface by supplying 3.3V to the VIO pin. The target pre-stage interface terminal is the SCK / CSn / SI / OMODE input pin and SO output pin in 4-wire CMOS mode.

When the host device, which is directly connected to the pre-stage interface, is a 5V system, the VIO pin is shorted to VREG5 pin over the substrate. In this case, the pre-stage interface pin operates on a 5V system (using VREG5 power supply).

Power Down (PDWN)

This product can be changed to a low power state (power down) on setting the PDWN pin to High level. The internal circuit gets reset on setting this pin to High level and the resistor and internal step change reverts to the initial state. All driver outputs change to OFF.

In the case of using this pin as a reset pin, the condenser connected to VREG5 is discharged and hence, it is recommended that the PDWN pin be kept at High level for about 100ms. If the discharging of the condenser is inadequate, an operation such as an unstable interface output may occur temporarily.

Internal Oscillator Frequency Select (ROSC)

This device contains an oscillator for internal logic circuit.
This pin is usually connected to GND with a 47kohm pull-down resistor for the oscillator reference current.

FAULTn Pin

The FAULTn pin outputs Low level at the time of detecting Over Current Protection function (OCP) and detecting Thermal Shutdown function (TSD). It generally becomes an open drain output and becomes High-Z. In the case of using this pin for detection of abnormalities, use this by pulling up to the power supply line below 5V.

Driver Operation Mode

The operation mode of the stepping motor control can be selected by setting DMODE pin. Perform the settings as set out in the table below according to the operation mode to be used.

Table 15. Operation Mode (DMODE) Setting

DMODE	Description
0	Phase input mode
1	Clock input mode

[Phase input mode]

Functions as phase input mode based on fixing the DMODE pin to Low level. In phase input mode, the value set in the register is directly reflected on output.

[Clock input mode]

Functions as clock input mode based on fixing the DMODE terminal to High level. In the clock input mode, internal step advances and output is changed according to the step when CK bit changes from 0 to 1. Step direction and excitation mode can be selected by the PEM bit. The excitation mode corresponds to phase 1 excitation / phase 2 excitation / phase 1-2 excitations. For resistor details, see the **Register Map** section.

* The behavior in the case of change-over of mode during operation cannot be guaranteed.

Functional Description (continued)

ODSDRn Pin Settings

In case of using the multi-drop connection, the sensor can be used based on setting SDR_OUT of the post-stage device as open drain and setting SDR_IN input of the pre-stage device as pull-up.

SDR_OUT output pin becomes the open drain output by fixing the ODSDRn pin to Low level. Set the pull-up as ON in register settings (SDR_PUPn=0) in the opposite pre-stage device.

When connection with a pre-stage device becomes the cascade connection (1:1), fix the ODSDRn pin to High level and use it as a push-pull output. It is recommended that at this time the pull-up be set to OFF in the register settings of the pre-stage device, since the electricity consumption for Low level output lowers.

Address specification mode can be used at the time of multi drop connection. See the **Communication Protocol** section described below) and shift resistor mode cannot be used.

Device Address Setting

The least significant 5 bits out of the device address 8 bits of the serial interface are set using pins A0 to A4. The most significant 3 bits are fixed to 3'b010 and these are classified as the communication for the LED driver LSI THL35XX series (most significant 2 bits are 2'b00) made by our company.

Table 16. Device Address Setting

Pin setting								Device operation
(Internal fix)			A4	A3	A2	A1	A0	
0	1	0	0	0	0	0	0	Only work with broadcast address mode
			0	0	0	0	1	Work with broadcast and address assign mode. (Please use it within this range.)
			1	1	1	1	0	
			1	1	1	1	1	Register write-protected (use of repeater)
0	0	A5 – A0						(Ref.) LED driver THL35xx series

(Setting example) In the case of terminals A4=Low, A3=Low, A2=Low, A1=Low, A0=High,
The device address is set to 8'b01000001 (=8'h41).

When all pins A0 to A4 are set to High level (device address 8'b01011111=8'h5F), register writing on this device is disabled. In the case of using only 3-wire CMOS → 3-wire CMOS repeater function or 4-wire CMOS → 3-wire CMOS bridge function without using the motor driver output of the wire bridge function, set all A0 to A4 to High level.

The device address 8'b01000000 (=8'h40) becomes the device address for writing on all the connected motor drivers (broadcast). When all A0 to A4 are set to Low level, the device operates only by broadcast specification. Set the device address within the range from 8'b01000001 (=8'h41) to 8'b01011110(=8'h3E).

Register Map

This product controls the operation of the output transistor by setting a value in the internal register using serial communication. The function differs depending upon the operation mode and hence, check the mode that is set at the external pin (DMODE) in the following table.

Table 17. Register Map

(a) Phase input mode (DMODE = "Low")

Register address (Run command)	Bit	Default	Function	Description
8'h00	7	0	SDR_PUPn	SDR_IN(*1) Pull-up setting 0:ON 1:OFF
	6	0	Reserved	Reserved bit Please usually set to "0".
	5	0	BLANK_EN	Blank function setting Please usually set to "1".
	4	0	BLANK_SEL	Blank time driver ON 0:1CLK 1:3CLK Setting(*2) driver OFF 0:2CLK 1:4CLK
	3	0	IN_B1	OUTB1 Output transistor 0:ON 1:OFF
	2	0	IN_B0	OUTB0 Output transistor 0:ON 1:OFF
	1	0	IN_A1	OUTA1 Output transistor 0:ON 1:OFF
	0	0	IN_A0	OUTA0 Output transistor 0:ON 1:OFF

(b) Clock input mode (DMODE = "High")

Register address (Run command)	Bit	Default	Function	Description
8'h00	7	0	SDR_PUPn	SDR_IN(*1) Pull-up setting 0:ON 1:OFF
	6	0	Reserved	Reserved bit Please usually set to "0".
	5	0	BLANK_EN	Blank function setting Please usually set to "1".
	4	0	BLANK_SEL	Blank time driver ON 0:1CLK 1:3CLK Setting(*2) driver OFF 0:2CLK 1:4CLK
	3	0	PEM	Set the excitations 2'b00: All output OFF 2'b01: 1phase excitation 2'b10: 2phase excitation 2'b11: 1-2phase excitation
	2	0		
	1	0	CW/CCW	Set the direction of step.(*2) 0: CW 1: CCW
	0	0	CK	Advance the internal step. 0 → 1: Advanced step other: kept step

(*1) The pin name varies depending upon the output mode. For details, see the Pin List.
In case of LVDS output, the SDR_INp pin is used as an internal pull-up and the SDR_Inn pin is used as pull-down.
In the case of CMOS output, the SDR_IN pin is used as an internal pull-up.
(*2) CLK that becomes the standard of blank time becomes the internal OSCCLK (typ. 1.6MHz).
(*3) For details of the output transistor operation by step forward direction settings, see the items of [Clock Input Mode] of **Driver Operation Mode**.

Communication Protocol

The serial communication of this product is controlled by the following protocol.

Table 18. Communication Protocol

Byte Number		Bit Number								Data direction
		7	6	5	4	3	2	1	0	
0	Data type	Device address								↓
	IN	0	1	0	A4	A3	A2	A1	A0	↓
	OUT	-	-	-	-	-	-	-	-	↓
1	Data type	Run command								↓
	IN	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	↓
	OUT	-	-	-	-	-	-	-	-	↓
2~	Data type	Read and write data								↓
	IN	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	↓
	OUT	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	↓

The serial interface is a clock synchronization system, which performs writing in register and reading of sensor signals (GPIN3 to GPIN0 pin input).
In the case of consolidating GPIN3 to GPIN0 pins to 4-bit, this has been denoted below as “GPIN Pin”.

- The data length is 8-bit and MSB is first. For the specification method of the header bit (Header Condition), see the **Electrical Characteristics** section.
- The first 8-bit including the header bit are denoted as “byte 0” and the next 8-bit are denoted as “byte 1”.
- The address of the device that carries out the communication is specified by byte 0. All devices (only motor driver) are accessed on specifying the device address at 8’h40.
  Here, the device for which device address is set as 8’h5F at the pins A4 to A0 is excluded.
- Execution command is specified by byte 1. For execution command, see Table 19.
- Byte 2 onwards is writing and reading data. The content of write/read data vary depending upon the execution command specified by byte 1. Hence, check the details for each command.

Table 19. Command Descriptions

write to register	Command		Run		
	HEX	BIN	write register	read sensor signals (GPIN pin data)	
				address assign mode	shift register mode
write register	8’h00	8’b00000000	○	×	×
read sensor signals (address assign mode)	8’h88	8’b10001000	×	○	×
write register / read sensor signals (address assign mode)	8’h80	8’b10000000	○	○	×
read sensor signals (shift register mode)	8’hAA	8’b10101010	×	×	○

Do not specify the commands other than those given above.
If not particularly specified in this paragraph, the communication protocol/data example is seen from the host (CPU, microcontroller).

Serial interface Connections

[Cascade Connection]

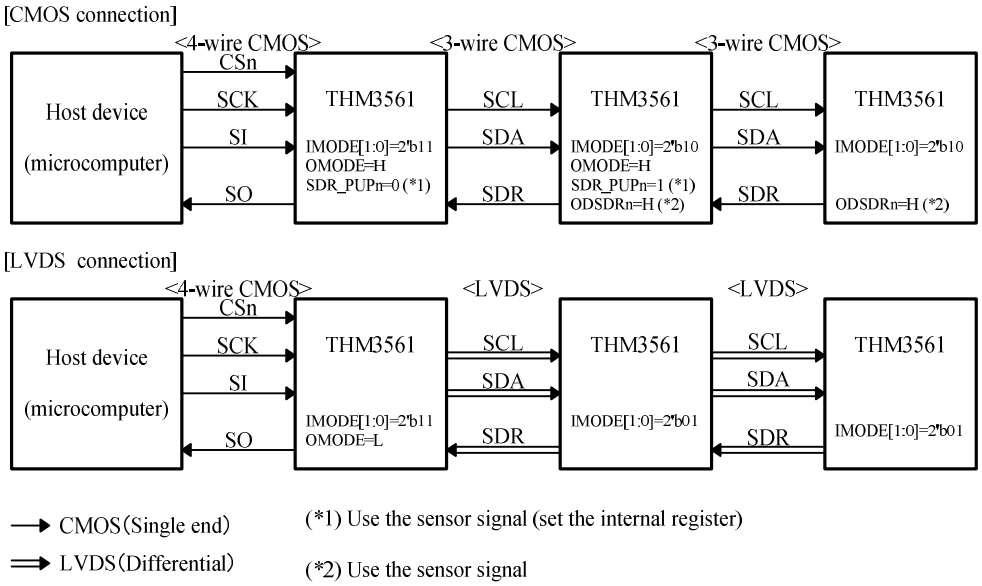


Figure 11. Cascade Connection

[Multi-drop Connection]

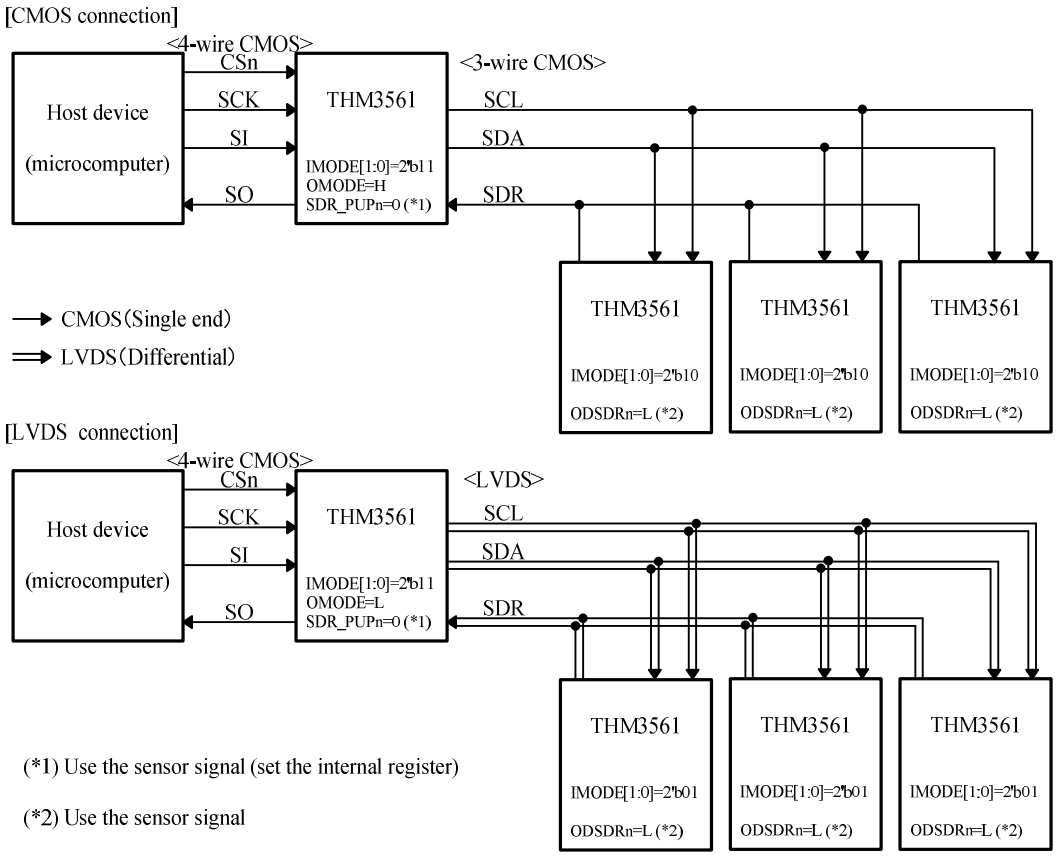


Figure 12. Multi-drop Connection

Serial Interface Connections (continued)

[Cascade and multi-drop connection]

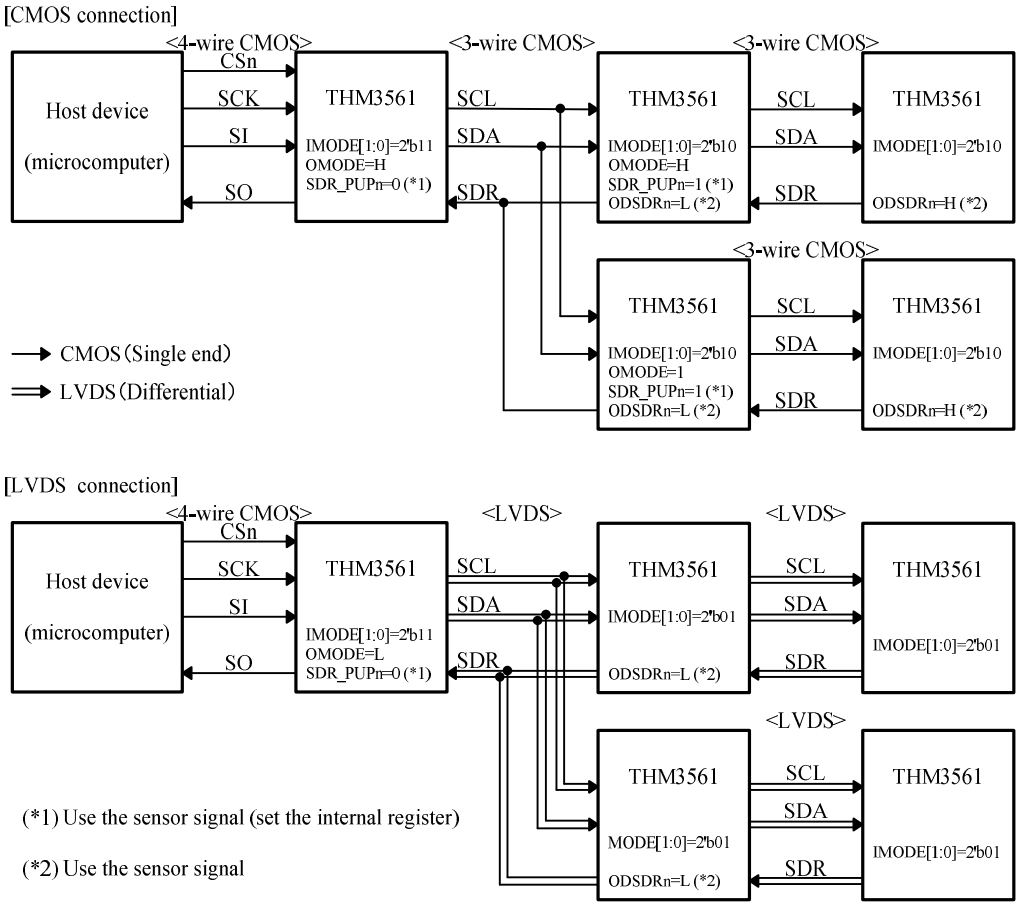


Figure 13. Cascade and Multi-drop Connection

Only address specification mode can be used for sensor signals in the case of multi-drop connection and cascade / multi-drop mixed connection. In the case of using sensor signals, set the SDR_OUT output to which plurality of devices are connected, to open drain mode (ODSDRn pin ="L"). Also, set the SDR_IN input of the opposite device to internal pull-up ON (SDR_PUPn register = "L").

In the case of using sensor signals for multi-drop connection (including mixing with cascade connection), the transfer rate lowers drastically for CMOS connections when compared to the LVDS connection. In the case of selecting this configuration, the use of LVDS connection is recommended. For details on communication rate etc., see application note.

Package

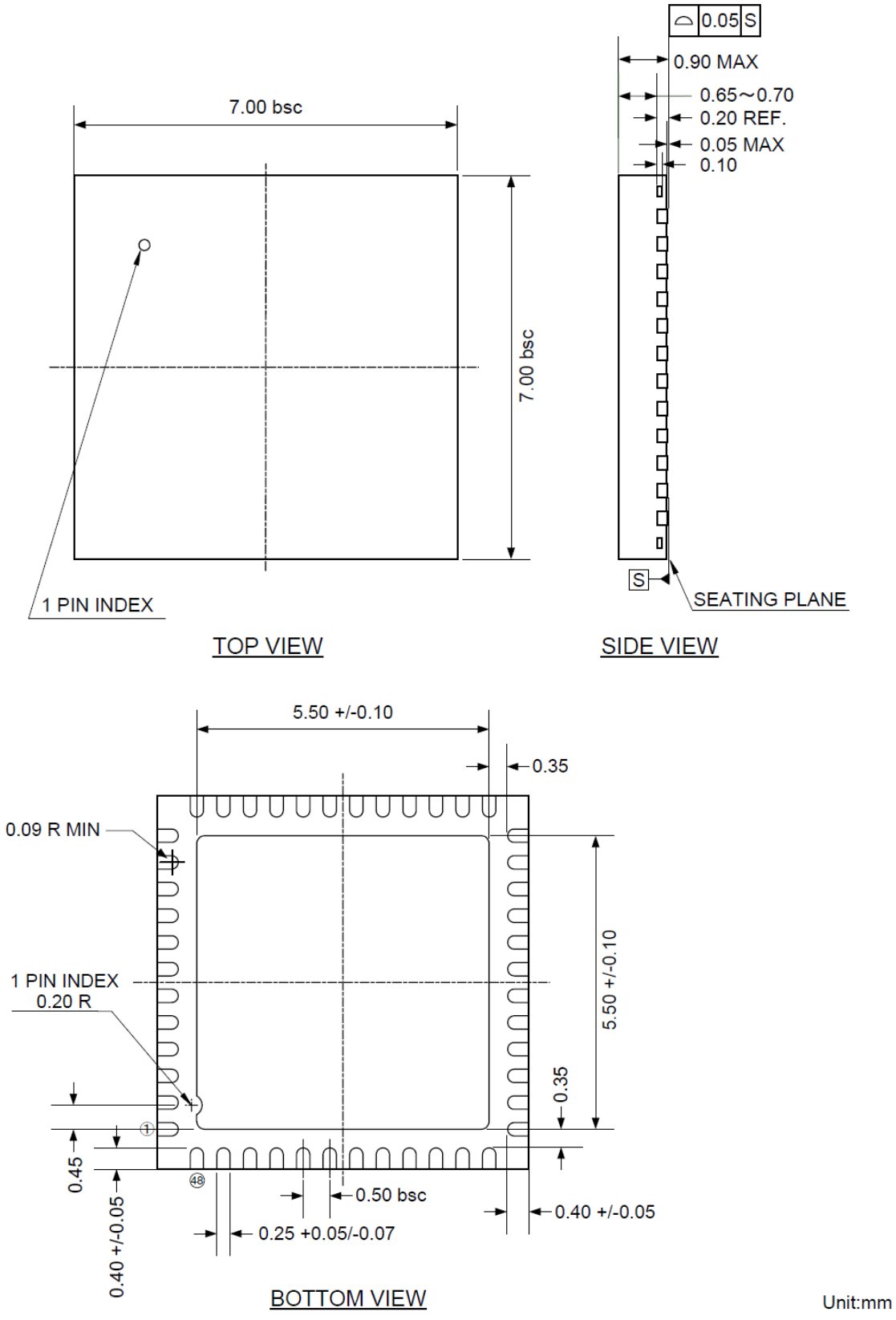


Figure 14. Package

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
3. This material contains our copyright, know-how or other proprietary. Copying or disclosing to third parties the contents of this material without our prior permission is prohibited.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
9. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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